forming on the thin region may further include selectively depositing resist over the thick region including the portion of unmasked epitaxial silicon remaining after the initial etch (thereby providing a pattern for a slab for photonics in the thick region), performing a remainder of the initial etch to remove unmasked portions of the remaining epitaxial silicon of the thick region, thereby defining a slab for photonics, and then stripping the resist deposited over the thick and thin regions. In one such specific case, forming on the thick region and forming on the thin region further include performing liner oxidation so that remaining epitaxial silicon is provided with an oxide layer. In another such specific case, forming on the thick region further includes carrying out a slab implant process. In another such specific case, forming on the thick region and forming on the thin region further include performing an oxide fill process to fill one or more shallow trench isolation regions, patterning an oxide thinning mask (thereby protecting the thick region and exposing the thin region), and then performing an oxide etch to remove a bulk of oxide above the thin region and any unprotected isolation region. Here, forming on the thick region and forming on the thin region may further include performing a chemical mechanical polish (CMP) process so as to polish all oxide down to the underlying top layer of nitride, and then removing remaining nitride. In one such case, forming on the thick region and forming on the thin region further include performing CMOS processing, such as sacrificial oxide growth, body implants, gate oxide growth, polysilicon gate deposition and patterning, dielectric spacer deposition and etch back, and/or source/drain implants.

[0010] The features and advantages described herein are not all-inclusive and, in particular, many additional features and advantages will be apparent to one of ordinary skill in the art in view of the drawings, specification, and claims. Moreover, it should be noted that the language used in the specification has been principally selected for readability and instructional purposes, and not to limit the scope of the inventive subject matter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIGS. **1-14** show a series of cross-sectional side-views that illustrate a method for fabricating a semiconductor having structures and devices of varying thickness, as well as the resulting semiconductor itself, in accordance with an embodiment of the present invention. Note that the figures are not drawn to scale; rather, they are drawn to facilitate explanation. Details such as layer thicknesses and actual section or feature locations will be apparent from the corresponding detailed description.

DETAILED DESCRIPTION OF THE INVENTION

[0012] Techniques are disclosed that facilitate the fabrication of semiconductors including structures and devices of varying thickness. For instance, the techniques can be used to fabricate silicon circuitry that includes fully depleted silicon-on-insulator (SOI) devices (e.g., around 500 A Si thickness), photonic waveguides (e.g., around 2300 A Si thickness), and/or ring modulators (e.g., which may have slab thickness values around 500 to 800 A). Likewise, the techniques can be used to fabricate silicon-based circuitry that includes both channel and ridge waveguide structures. Semiconductor circuitry fabricated with materials other than silicon (e.g., gallium arsenide, indium phosphate, and quartz, sapphire) can equally benefit from the techniques, and numerous circuit configurations will be apparent in light of this disclosure. The techniques are not intended to be limited to particular semiconductor materials or specific types of circuitry/structures; rather, any semiconductor materials that can be configured with circuitry/structures of varying thickness may benefit.

[0013] General Overview

[0014] As previously explained, semiconductors including both CMOS circuitry and silicon waveguides are currently fabricated so that the CMOS circuitry and waveguides essentially have the same silicon thickness. Such conventional techniques are associated with a number of disadvantages, including that they do not allow for fully depleted SOI devices. Nor do they allow for the ability to modify waveguide thickness independently of the CMOS devices.

[0015] One embodiment of the present invention provides a method for fabricating SOI CMOS devices and silicon high index contrast (HIC) silicon waveguides and photonic devices on the same substrate, where at least one of the CMOS devices has a silicon thickness that is significantly thinner than the silicon thickness for the silicon waveguides. In some specific such embodiments, the method may be used for integration of fully depleted CMOS devices with silicon HIC waveguides having channel and ridge type configurations.

[0016] The method may employ a substrate having epitaxial silicon on buried oxide, although other suitable substrate materials and configurations can be used, as will be apparent in light of this disclosure. The method of this example embodiment generally includes thinning the silicon in the fully depleted CMOS region before beginning the patterning and formation of the silicon waveguides, and before creating isolation regions in the fully depleted CMOS regions. The silicon in the fully depleted CMOS region can be thinned, for instance, by completing pad oxidation, pad nitride deposition, photolithography to block (protect) the photonic regions, and patterning a nitride/oxide stack (also referred to as pad oxide and pad nitride layers, or collectively as a two-layer hardmask) to expose the silicon regions to be thinned.

[0017] Once the nitride/oxide stack is patterned as desired, one option is to implant oxygen into the silicon using the resist/nitride/oxide stack as a mask, and then strip the resist (note that resist can be stripped before or after implant process), wafer clean, and anneal to form oxide in the implanted regions. A second option is to dry etch the silicon to a desired depth, strip the resist (note that resist can be stripped before or after dry etch process), and complete a short oxidation to remove dry etch damage. A third option is to strip the resist, wafer clean, and then complete a thermal oxide growth to consume underlying silicon.

[0018] With any of these options, the next step of this example embodiment is to strip the nitride and oxide layers (or what remains thereof), which can be done, for example, using hot phosphoric acid and hydrofluoric acid, respectively. At this point, the waveguides can be formed while simultaneously patterning the thinned silicon region. One example process that can be used in forming waveguide structures including channel and ridge configurations is described in the previously incorporated U.S. application Ser. No. 12/201,807. Any waveguide slab regions may be implanted as needed. The trenches or spaces between silicon regions can then be filled, for example, with an oxide. In such cases, the resulting oxide layer is then planarized.